INFORMATION DISCLOSURE STATEMENT	Applicants	Takehiko HOJO
	Application No.	Not yet assigned
	Filed:	March 24, 2004
	For:	Semiconductor Integrated Circuit Provided With Semiconductor Memory Circuit Having Redundancy Function And Method For Transferring Address Data
	Group Art Unit:	Not yet assigned
	Examiner:	Not yet assigned
	Attorney Docket No.:	2102475-992040

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56(a) and 37 C.F.R. § 1.97, Applicant(s) hereby make of record the references listed on the accompanying Form PTO-1449 for consideration by the Examiner in connection with the examination of the above-identified patent application.

This Information Disclosure Statement:

(a)	☒	accompanies a new patent application submitted herewith.
(b)	☐	is filed within three (3) months of the Filing Date or before the mailing date of a First Office Action on the merits; OR
(c)	☐	after the period defined in (b) but before the mailing date of a Final Rejection or Notice of Allowance, OR
(d)	☐	is filed after the first Office Action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned prior to the mailing date of either a final rejection or a notice of allowance, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) or a certification as specified in 37 CFR § 1.97(e), as checked below OR
(e)	☐	is filed after the mailing date of either a final rejection or a notice of allowance, and the issue fee has not been paid, and is accompanied by the requisite petition fee ($130) set forth in 37 CFR § 1.17(l)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

As required under § 1.97(e), Applicants, through the undersigned, hereby state either that [check the appropriate space]:

(f)	☐	Each item of information contained in the Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing date of the Information Disclosure Statement; or

(g)	☐	No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

It is respectfully requested that each of the references shown on the attached Form PTO-1449 be made of record in this application. Copies of references are enclosed.

The Japanese Patent Application No. 2000-182394, as listed on the attached Form 1449, pertains to a conventional semiconductor memory device that has a redundancy function of replacing a regular memory cell with a spare memory cell when the regular memory cell is defective.

The Commissioner is authorized to charge any deficiencies and credit any overpayment of fees to our Deposit Account No. 07-1896.

Respectfully submitted,

Date: March 24, 2004

GRAY CARY WARE & FREIDENRICH LLP

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as EXPRESS MAIL (EV 302280479 US) in an envelope addressed to: Commissioner of Patents & Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450.

March 24, 2004 — *Date*

Marian Pirigyi — *Signature*

Form PTO-1449 (modified 2/91) U.S. DEPT. OF COMMERCE Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Attorney Docket Number: **2102475-992040**	Serial Number: Not yet assigned
	Applicants: Hojo, et al.	
	Filing date: March 24, 2004	Group art unit: Not yet assigned

U.S. PATENT DOCUMENTS

Examiner Initial	Patent number	Date	Name	Class	Sub-class	Filing date if appropriate

FOREIGN PATENT DOCUMENTS

	Document number	Date	Country	Class	Sub-class	Translation YES	NO
	2000-182394	6-30-2000	Japan				X

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Ouellette, et al, "Shared Fuse Macro for Multiple Embedded Memory Devices with Redundancy," IBM, Microelectronics Division, ASIC Development, Essex Junction, VT 05452, US, 4 pages, 2001 IEEE.

Examiner:	Date Considered:
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP '609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.	